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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/730,389	12/05/2003	James R. Lundberg	CNTR.2116	2619

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EXAMINER	
LE, DON P	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/730,389	LUNDBERG, JAMES R.	
	Examiner	Art Unit	
	Don P. Le	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9, 11-14, 18-22, 24-27* is/are rejected.

7)☐ Claim(s) *10,15-17 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 12/5/03, 5/8/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Kawasumi (US 6,127,862).

3. With respect to claim 1, figures 7 and 8 of Kawasumi disclose an output driver impedance controller that controls pull-down impedance of at least one output based on a reference value, comprising:

a programmable reference impedance generator (9) that develops reference impedance controlled by reference impedance control input (1);

at least one output driver (FIG. 8), each including a programmable output impedance generator coupled to a corresponding output and controlled an output impedance control input; and

an impedance matching controller (11) that continually adjusts said reference impedance control input to match said reference impedance with the reference value within a predetermined tolerance and that generates said output impedance control input based on said reference impedance control input.

4. With respect to claims 2 and 3, figures 7 and 8 of Kawasumi teaches said programmable reference impedance generator and each of said at least one programmable output impedance generator comprises a binary array of matched impedance devices (Q11-Q13, Q1-Q6).

5. Claims 1-9, 11-14, 18-22 and 24-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Shu et al. (US 5,457,407).

6. With respect to claim 1, figure 3 of Shu discloses an output driver impedance controller that controls pull-down impedance of at least one output based on a reference value, comprising:

a programmable reference impedance generator (comparator of figure 2, also see column 4, lines 5-10) that develops reference impedance controlled by reference impedance control input (vzqref);

at least one output driver (Q6-Q10), each including a programmable output impedance generator coupled to a corresponding output and controlled an output impedance control input; and

an impedance matching controller (Q1-Q5) that continually adjusts said reference impedance control input to match said reference impedance with the reference value within a predetermined tolerance and that generates said output impedance control input based on said reference impedance control input.

7. With respect to claims 2, 3 and 18, figure 3 of Shu teaches said programmable reference impedance generator and each of said at least one programmable output impedance generator comprises a binary array of matched impedance devices (Q11-Q13, Q1-Q6).

8. With respect to claims 4 and 19, figure 3 of Shu teaches said impedance matching controller comprises:

a voltage sensor (comparator of Figure 2) that senses a voltage difference between a reference voltage based on an input bus voltage and a voltage of said programmable reference impedance generator and that asserts an error signal indicative thereof; and

impedance control logic (NOR2) that adjusts said reference impedance control input based on said error signal.

9. With respect to claims 5 and 13, figure 3 of Shu teaches the reference value comprises reference resistor (R4), and wherein said input bus voltage (VCC) applied across said reference resistor and said programmable reference impedance generator coupled in series.

10. With respect to claims 6 and 20, figures 2 and 3 of Shu teach said impedance control logic receives a clock signal (10) and increments or decrements said reference impedance control input during selected cycles of said clock signal.

11. With respect to claim 7, figure 2 of Shu discloses bias adjustment logic (6) that combines a bias amount with said reference impedance control input to provide said output impedance control input.

12. With respect to claim 8, figures 2 and 3 of Shu disclose output bias logic (Q1-Q5) that is programmed to provide said bias amount.

13. With respect to claim 9, figures 2 and 3 of Shu disclose a first controller (line connected to external R4 to circuit) for coupling to an external reference resistor that provides a first reference value; and

a second controller (line connected to R3 to connected to circuit) including an internal reference resistor (R3) that provides a second reference value.

14. With respect to claim 11, figure 3 of Shu teaches output enable logic (OLB).

15. With respect to claim 12, figure 2 and 3 of Shu disclose a circuit, comprising:

a plurality of pins including a first reference pin (pin connected to one end R4) for receiving a reference voltage and at least one output pin (DQ);

at least one output driver (Q6-Q10), each including a programmable output impedance generator (NOR2) controlled by an output impedance control input (zqbit) and coupled to drive a corresponding one of said at least one output pin; and

impedance matching logic, comprising:

a programmable reference impedance generator (vzqref feedback to logic of figure 2) controlled by a reference impedance control input;

comparator logic (6) that continually adjusts said reference impedance control input to equalize values of a reference resistor coupled said first reference pin and said programmable reference impedance generator within a predetermined tolerance; and

output logic (12) that controls said output impedance control input based on said reference impedance control input.

16. With respect to claim 14, figure 3 of Shu discloses a second reference pin (the second end connected to R4) coupled to said programmable reference impedance generator and for coupling to one end of said reference resistor comprising an external reference resistor having its other end coupled to said first reference pin.

17. With respect to claims 21, 22 and 24-27, the methods therein are inherent given the apparatus of Shu as shown in the above rejections.

Allowable Subject Matter

18. Claims 10, 15-17 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

19. The following is an examiner's statement of reasons for allowance:

20. With respect to claims 10 and 23, the prior art does not teach a detection logic that monitors said reference impedance control input to determine whether said first reference value is coupled and that enables said second controller said first reference value is not coupled.

21. With respect to claim 15, the prior art does not teach an internal reference resistor connected in series with the external resistor.

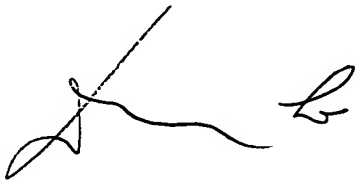
Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Don P. Le whose telephone number is 571-272-1806. The examiner can normally be reached on 7AM - 5PM.

22. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

5/25/2005



DON LE
PRIMARY EXAMINER